ISSN:0975-9646

Analysis of Fast FIR Algorithms based Area Efficient FIR Digital Filters

Shikha Jain
PG Student/VLSI Design

Prof. Ravi Koneti
Professor

Dr. Rita Jain
HoD of ECE

Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, India

Abstract*:- *In digital systems, the filters occupy a major role. This paper reviews several techniques used for designing & implementing low power area efficient digital filters & it presents the methods to reduce dynamic power consumption of a digital Finite Impulse Response (FIR) filter. This work describes the design of parallel FIR filter structures using polyphase decomposition technique, that requires minimum number of multipliers and low power adders. Normally multipliers consume more power and large area than the adders. For reducing the area, this filter structure uses adders instead of multipliers since the adder requires low power and less area than the multipliers. Moreover, number of adders does not increase along with the length of parallel FIR filter. This paper reviews those techniques, which saves the multipliers, for example for a 3 parallel 27 tap FIR filter saves 8 multiplier and 3 parallel 147 tap FIR filter saves 48 multipliers. The FIR filter was synthesized implemented using Xilinx ISE V10.1 and Virtex IV FPGA to target device xc3s250e.

Keywords:- **Fast Finite-impulse response (FIR) algorithms (FFAs), Digital Signal Processing(DSP), Parallel FIR.**

I. INTRODUCTION

Digital signal processing(DSP) has many advantages over analog signal processing. Digital signals are more robust than analog signals with respect to temperature and process variations. The FIR digital filter is one of most widely used fundamental devices performed in DSP systems. In a typical digital filtering application, software running on a digital signal processor (DSP) reads input samples from an A/D converter, performs the mathematical manipulations dictated by theory for the required filter type, and outputs the result via a D/A converter. Many algorithms are known to reduce the arithmetic complexity of FIR filtering.

Finite-Impulse Response (FIR) filters have been and continue to be important building blocks in many digital signal processing (DSP) systems. Due to the increase of portable battery-powered wireless systems in recent years, such as cellular phones and pagers, low power and small area digital filter designs have become more and more important.

There have been a few papers proposing ways to reduce the complexity of the parallel FIR filter in the past. In [1]–[4], poly phase decomposition is mainly manipulated, where the small-sized parallel FIR filter structures are derived first and then the larger block-sized ones can be constructed by cascading or iterating small-sized parallel FIR filtering blocks. In [5]–[7], the fast linear convolution is utilized to develop the small-sized filtering structures and then a long convolution is decomposed into several short convolutions, i.e., larger block-sized filtering structures can be constructed through iterations of the small-sized filtering structures. However, in both categories of method, when it comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration for the design of structures yet, which can lead to a significant saving in hardware cost. In this paper, we provide new parallel FIR filter structures based on FFA consisting of advantageous poly phase decompositions, which can reduce amounts of multiplications in the sub filter section by exploiting the inherent nature of the symmetric coefficients, compared to the existing FFA fast parallel FIR filter structure.

Fast FIR algorithms (FFAs) introduced in [1]–[3] show that they can implement an L-parallel filter using approximately $(2L-1)$ subfilter blocks, each of which is of length N/L. It reduces the required number of multipliers to $(2N-N/L)$ from $L \times N$. In [5]–[9], the fast linear convolution is utilized to develop the small-sized filtering structures, and then a long convolution is decomposed into several short convolutions. However, in both categories of methods, when it comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration yet, which can lead to a significant saving in hardware cost. Previously, we have investigated the design for symmetric convolutions based on even length [10]. In this brief, we will discuss symmetric convolutions based on odd length and provide new parallel FIR digital filter architectures consisting of advantageous polyphase decomposition, which can further reduce amounts of multipliers required in the subfilter section by exploiting the inherent nature of the symmetric coefficients, compared with the existing FFA fast parallel FIR filter structures. This brief is organized as follows.

A large amount of work has addressed the use of efficient implementations of multiplier-less MCMs. The techniques include the use of different number representation schemes, the use of different architectures and implementation styles and the coefficient optimization techniques, e.g., [1-8]. Most of these work use heuristic algorithms to minimize the total number of adders/subtractors in the multiplier blocks of the filters.

II. OVERVIEW OF THE FFA ALGORITHM

With the continuing trends to reduce the chip size and integrates multichip solution into a single chip solution it is important to limit the silicon area required to implement parallel FIR digital filter in VLSI implementation. The Need for high performance and low power digital signal processing is getting increased. Finite Impulse Response (FIR) filters are one of the most widely used fundamental devices performed in DSP system.

A. ***General Form(Traditional Algorithm)***

Consider an N-tap FIR filter which can be expressed in the general form as

$$Y_n = \sum_{i=0}^{N-1} h_i x_{n-i}, \quad n=0,1,2,\ldots,\infty \quad (1)$$

Where {x (n)} is an infinite-length input sequence and {h (i)} are the length-N FIR filter coefficients. This block FIR filtering equation shows that the parallel FIR filter can be realized using *L*2-FIR filters of length *N/L*. This linear complexity can be reduced using various FFA structures.

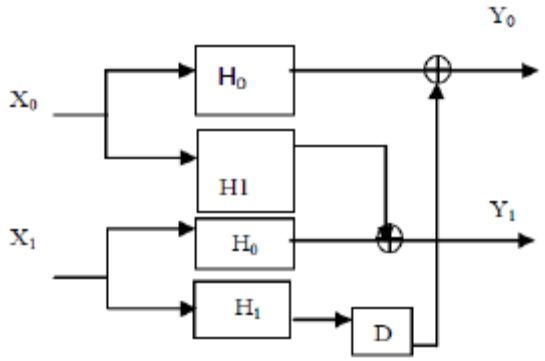

Fig. 1 Traditional 2X2 Parallel FIR filter Implementation

B. ***First Approach***

1) 2 X 2 FFA-1 approach (L = 2)

According to polyphase decomposition, a two-parallel FIR filter can be expressed as

$$Y_0 + Z^{-1}Y_1 = (H_0 + Z^{-1}H_1)(X_0 + Z^{-1}X_1)$$
$$= H_0 X_0 + (H_0 X_1 + H_1 X_0)Z^{-1} + H_1 X_1 Z^{-2} \quad (2)$$

which implies that,

$$Y_0 = H_0 X_0 + Z^{-2}H_1 X_1$$
$$Y_1 = H_0 X_1 + H_1 X_0 \quad (3)$$

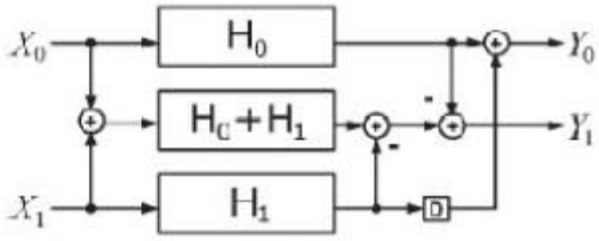

Fig. 2 First Approach 2 Parallel FIR filter Implementation

However, (3) can be written as

$$Y_0 = H_0 X_0 + Z^{-2}H_1 X_1$$
$$Y_1 = (H_0 + H_1)(X_0 + X_1) - H_1 X_1 - H_0 X_0 \quad (4)$$

The (2X2) FFA results in a filtering structure are shown in figure 2. At first it may seem that (2X2) uses 5 filtering operations since Y0 requires 2 multipliers (filtering operations) and *Y1* requires 3 multipliers. However, *X0H0* and *X1H1* are found in both *Y0* and *Y1*. These two terms need only to be computed once which means that the total number of filtering operations is 3. This means that the (2X2) FFA structure uses 3(*N*/2) multipliers and 3(*N*/2–1)+4 adders.

2) 3X3 FFA-1 Approach

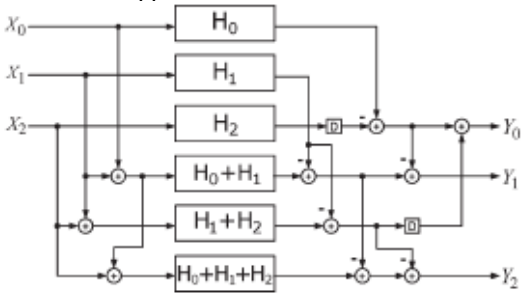

Fig.3 First Approach 3 Parallel FIR filter Implementation

By the similar approach, a three-parallel FIR filter using the FFA can be expressed as [1], [3]

$$Y0 = H0X0 - z^{-3} H2X2 + z^{-3} \times [(H1 + H2)(X1 + X2) - H1X1]$$
$$Y1 = [(H0 + H1)(X0 + X1) - H1X1] - (H0X0 - z^{-3}H2X2)$$
$$Y2 = [(H0 + H1 + H2)(X0 + X1 + X2)] - [(H0 + H1)(X0 + X1) - H1X1] - [(H1 + H2)(X1 + X2) - H1X1] \quad (5)$$

C. ***Second Approach***

1) 2X2 FFA-2 Approach

When it comes to a set of even symmetric coefficients, this can earn one more subfilter block containing symmetric coefficients than (3), the first FFA approach parallel FIR filter. Fig. shows implementation of the this two-parallel FIR filter.

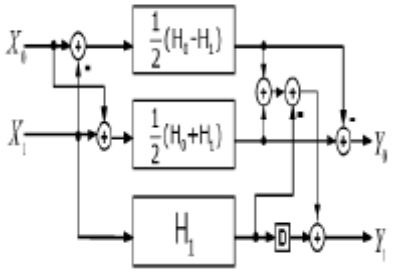

Fig.4 Second Approach23 Parallel FIR filter Implementation

2) 3X3 FFA-2 Approach

To exploit the symmetry of coefficients, the main idea is to manipulate the polyphase decomposition to earn as many subfilter blocks as possible, which contain symmetric coefficients so that half the number of multipliers within a single subfilter block can be utilized for the multiplications of whole taps.

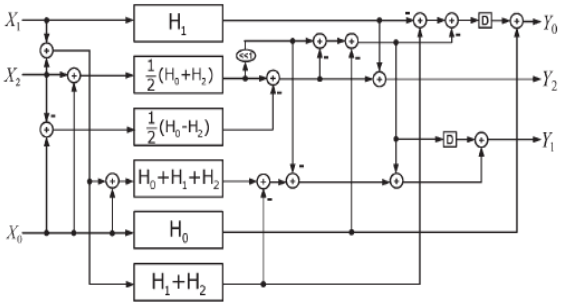

Fig.5 Second Approach 3 Parallel FIR filter Implementation

$$Y0 = H0X0 + z^{-3} \times \{ (H1 + H2)(X1 + X2) - H1X1 - [(H0 + H2)(X0 + X2) - H0X0 - \tfrac{1}{2} [(H0 + H2)(X0 + X2) - (H0 - H2)(X0 - X2)]\}$$

$$Y1 = (H0 + H1 + H2)(X0 + X1 + X2) - (H1+H2)(X1+X2) - (H0 + H2)(X0 + X2) + \{(H0 + H2)(X0 + X2) - 1/2 \times [(H0 + H2)(X0 + X2) - (H0 - H2)(X0 - X2)] - H0X0\} + z^{-3}\{ (H0 + H2)(X0 + X2) - \tfrac{1}{2} \times [(H0 + H2)(X0 + X2) - (H0 - H2)(X0 - X2)] - H0X0\}$$

$$Y2 = H1X1 + \tfrac{1}{2} \times [(H0+H2)(X0+X2) - (H0-H2)(X0-X2)] \quad (6)$$

Consider a 27-tap FIR filter with a set of sym- metric coefficients as follows:

h(0) = h(26), h(1) = h(25), h(2) = h(24), h(3) = h(23), h(4) = h(22), h(5) = h(21), . . .
, h(12) = h(14),
applying to the second structure, and then, we gain two more sub filter blocks with symmetric coefficients as

H0 ± H2 = {h(0) ± h(2), h(3) ± h(5), h(6) ± h(8), . . . , h(18)±h(20), h(21) ±
h(23), h(24) ± h(26)}
where h(0) ± h(2) = ± (h(24) ± h(26)) h(3) ± h(5) = ± (h(21) ± h(23))
h(6) ± h(8) = ± (h(18) ± h(20))

So that half the number of multipliers within a single sub filter block can be utilized for the multiplications of whole taps.

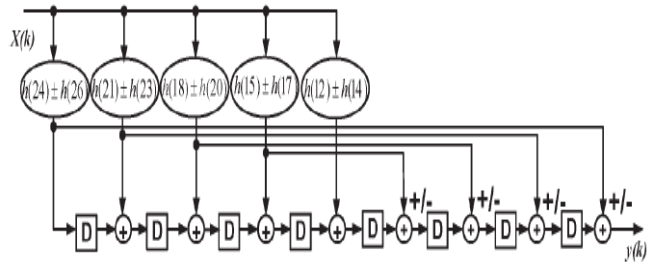

Fig.6 Implementation of sub filter blocks

As shown from the given example, after applying the second structure , in Fig. 5, four out of six subfilter blocks, i.e., *H*1, *H*0 + *H*2,H0-H2, *H*0 + *H*1 + *H*2, are with symmetric coefficients now, which means a single subfilter block can be realized in Fig. 6, with only half the amount of multipliers required. Each output of multipliers responds to two taps, except the middle one. Note that the transposed direct-form FIR filter is employed. Compared with the first structure FFA three-parallel FIR filter structure, the second structure leads to two more subfilter blocks, which contains symmetric coefficients.Therefore, for an *N*-tap three-parallel FIR filter, the second structure can save *N*/3 multipliers from the first FFA structure. However, it comes with the price of the increase in amount of adders, i.e., five additional adders, in preprocessing and postprocessing blocks.

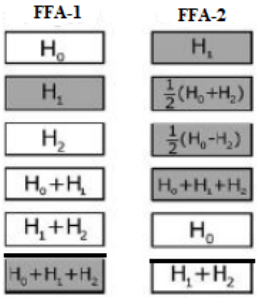

Fig. 7 Comparison between subfilter block of both structure

III. COMPARISON OF FIRST AND THE SECOND FFA STRUCTURES

COMPARISON OF FIRST AND THE SECOND FFA STRUCTURES NUMBER OF REQUIRED MULTIPLIERS (M.), REDUCED MULTIPLIERS (R.M.), NUMBER OF REQUIRED ADDERS IN SUBFILTER SECTION (SUB.), NUMBER OF REQUIRED ADDERS IN PRE/POSTPROCESSING BLOCKS (PRE/POST.), NUMBER OF THE INCREASED ADDERS (I.A.)

TABLE 1

L	Length	Structure	M.	R.M.	Required Adders		I.A.
					Sub.	Pre/Post.	
3	27-tap	FFA-1	46	8 (17.4%)	48	10	5
		FFA-2	38			15	
	81-tap	FFA-1	136	26 (19.1%)	156	10	
		FFA-2	110			15	
	147-tap	FFA-1	246	48 (19.5%)	288	10	
		FFA-2	198			15	
	591-tap	FFA-1	986	196 (19.9%)	1176	10	
		FFA-2	790			15	
4	27-tap	FFA-1	54	3 (5.6%)	63	20	4
		FFA-2	51			24	
	81-tap	FFA-1	159	10 (6.3%)	180	20	
		FFA-2	149			24	
	147-tap	FFA-1	279	18 (6.5%)	324	20	
		FFA-2	261			24	
	591-tap	FFA-1	1110	74 (6.7%)	1323	20	
		FFA-2	1036			24	
6	27-tap	FFA-1	82	6 (7.3%)	72	42	11
		FFA-2	76			53	
	81-tap	FFA-1	224	21 (9.4%)	234	42	
		FFA-2	203			53	
	147-tap	FFA-1	402	36 (9.0%)	432	42	
		FFA-2	366			53	
	591-tap	FFA-1	1586	147 (9.3%)	1764	42	
		FFA-2	1439			53	
8	27-tap	FFA-1	100	8 (8.0%)	81	80	16
		FFA-2	92			96	
	81-tap	FFA-1	277	20 (7.2%)	270	80	
		FFA-2	257			96	
	147-tap	FFA-1	477	36 (7.6%)	486	80	
		FFA-2	441			96	
	591-tap	FFA-1	1850	148 (8.0%)	1971	80	
		FFA-2	1702			96	

Another table for L=2 in length 1 tap, 9 tap, 27 tap and 81 tap as shown.

TABLE 2

L	Length	Structure	Used Multiplier	Reduced Multiplier	Required Adders		Increased Adders
					Subtractor	Pre /Post Process	
2	1 tap	FFA-1	3	-	2	5	3
		FFA-2	3			8	
	9 tap	FFA-1	27	6	18	45	27
		FFA-2	21			72	
	27 tap	FFA-1	81	8	54	135	81
		FFA-2	73			216	
	81 tap	FFA-1	243	24	162	405	243
		FFA-2	219			648	

IV. CONCLUSION

In this paper, we have reviewed parallel FIR filter structures, which are beneficial to symmetric convolutions when the number of taps is the multiple of 2 or 3. Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation. The SECOND structure exploits the nature of even symmetric coefficients and save a significant amount of multipliers at the expense of additional adders. Since multipliers outweigh adders in hardware cost, it is profitable to exchange multipliers with adders. Moreover, the number of increased adders stays still when the length of FIR filter becomes large, whereas the number of reduced multipliers increases along with the length of FIR filter. Consequently, the larger the length of FIR filters is, the more the second structures can save from the first FFA structures, with respect to the hardware cost. Overall, in this paper, we have provided new parallel FIR structures consisting of advantageous polyphase decompositions dealing with symmetric convolutions comparatively better than the first FFA structures in terms of hardware consumption. So, now apply this idea we can implement a new technique which reduces more multipliers and can reduces more system cost.

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